An Overview of Wide Bandgap Power Semiconductor Device Packaging Techniques for EMI Reduction

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***Abstract*— Wide band gap (WBG) power semiconductor devices have been increasingly desirable due to their superior characteristics compared to their Si counterparts. However, their faster switching speed and abilities to operate at higher frequency than Si devices have brought new challenges, among which Electromagnetic interference (EMI) issue is one of the major concerns. EMI issues in WBG device applications had been reported in many papers. However, package layout determined characteristics has not yet been connected to electromagnetic compliance (EMC) analysis. In this paper, characteristics of WBG power devices as EMI noise sources are investigated, package design considerations that could reduce EMI are reviewed.**

***Index Terms*—Electromagnetic interference, Wide bandgap devices, package design, Silicon carbide (SiC), Gallium nitride (GaN), power module**

I. Introduction

With the development of power electronics, the continuing demand of higher efficiency and higher power density design is pushing the performance of power semiconductors to the limit of Si material. At the same time, Wide Bandgap semiconductor materials including SiC and GaN, have presented multiple advantages over Si materials. Thus, wide bandgap (WBG) power devices have been an increasingly important role in power electronics systems [1] - [4]. As shown in Table I, WBG materials present higher critical electric field compared to Si, which enables higher breakdown voltage in the same size. In addition, the higher thermal conductivity of SiC improves high power operation performance. These material properties that used to impair the increasing of power density due to limitations of Si, have been greatly improved by WBG material.

With the commercialization of WBG power semiconductors [2], various applications utilizing WBG devices have proved to have improved behaviors including increased efficiency, achieved higher power density, and higher temperature withstand ability. However, the high dv/dt and di/dt [5] associated with faster switching speed and high frequency ringing during switching transient of WBG devices also increase the concern of conductive EMI [6] - [11], [13] - [16], near field coupling [18] - [22], and radiated EMI [20], [39]. As an inevitable part of design consideration, EMI issues must be addressed properly, otherwise the full benefits of WBG power devices will be compromised.

There are plenty of researches discussing EMI issues in systems with WBG devices, among which package improvements are the most straightforward method because the EMI would be reduced from the source. A systematic overview is conducted in this survey, state of the art EMI reduction methods focusing on package design for power electronics systems with WBG devices were reviewed.

II. EMI Related Characteristics of Popular WBG Power Switches

When analyzing power semiconductor devices switching behavior, the double pulse tester (DPT) with clamped inductive load circuit is widely used. As seen in Fig.1, a general double pulse tester with parasitic components included is showed. The freewheeling diode model consists of junction capacitor, ideal diode, and a series resistor. A MOSFET model is used as power switch, C_{GS}, C_{DS}, and C_{GD} are gate to source capacitor, drain to source capacitor and gate to drain respectively. Parasitic inductance L_d and L_s are drain inductance and source inductance, respectively. Gate inductance is ignored here because it is determined by driver design rather than device characteristics. In this DPT with clamped inductive load, the load inductance is assumed large enough to maintain constant current. So, it is replaced by a constant current source I_L.

TABLE I. Comparison of Material Properties [6]

Parameters	Si	SiC	GaN
Band Gap E_g (eV)	1.12	3.2	3.4
Critical Field E_{crit} (MV/cm)	0.3	3.5	3.3
Electron Mobility μ_n ($cm^2/(V\cdot s)$)	1500	650	990-2000
Permittivity ε_r	11.8	9.7	9
Thermal Conductivity (W/cm°C)	1.5	4.9	1.3
Saturation Drift Velocity (cm/s $\cdot 10^7$)	1	2.7	2.7

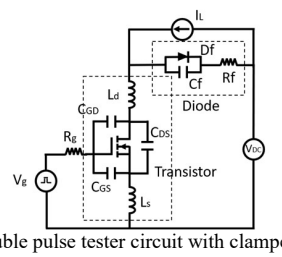


Fig. 1. Schematic of double pulse tester circuit with clamped inductive load

The V_{DC} represent the input voltage, it can be a battery or DC source, it provides constant voltage input.

A. Switching Characteristics of WBG Power Switches

The most popular power switches made with WBG materials are SiC MOSFETs [3] and GaN HEMTs [2]. Varies evaluations and applications have proved their better performance over Si MOSFETs and IGBTs. Although there are also applications using SiC JFETs, the undesirable normally-on characteristic of JFETs are limiting their performance.

Because of the higher critical field of Wide Bandgap material, as shown in Table I, under the same power rating, WBG power switches usually have smaller die size than their Si counterparts. Due to its structure, the capacitance of a power

transistor can be described by parallel plate capacitors. The capacitance can be calculated by (1).

$$C = \varepsilon_0 \varepsilon_r \frac{WL}{t} \quad (1)$$

Where ε_0 and ε_r are permittivity of the material, W and L are the width and length of the plate respectively, t is the thickness between the two plates. In power semiconductor devices, gate terminals are usually much closer to source pads, while drain terminals are separated from those two by drift regions to guarantee voltage blocking capability. Thus, based on (1), the gate to source capacitance C_{gs} should be much bigger than C_{gd} and C_{ds} due to smaller thickness. For WBG transistors, because the die sizes are much smaller than Si transistors, while the oxide thickness between gate and source does not vary much, C_{gs} of SiC MOSFET and GaN HEMT are much smaller than their Si counterparts. In high power applications, Si MOSFET would have to increase die size to prevent break down, thus, the output capacitance of Si MOSFET is also bigger than SiC MOSFET. For GaN HEMT, most of the applications are under 650 V power rating. The difference of die size between Si MOSFET and GaN HEMT is smaller than that between high power SiC MOSFET and Si MOSFET. Due to smaller drift region thickness, C_{ds} and C_{gd} of GaN HEMT are not reduced very much, even larger than those in Si transistors.

In Fig.1, when the gate signal is a step-up function, the drain current and drain to source voltage of the transistor could be expressed as (2) (3), when the gate signal is a step-down function, the drain current and drain to source voltage of the transistor could be expressed as (4) and (5) [31]:

$$\frac{dI_d}{dt} = \frac{V_g - (\frac{I_d}{g_m} + V_{th})}{R_g \frac{C_{iss}}{g_m} + L_s} \quad (2)$$

$$\frac{dV_{ds}}{dt} = -\frac{V_g - V_{Miller}}{R_g C_{gd}} \quad (3)$$

$$\frac{dI_d}{dt} = -\frac{\frac{I_d}{g_m} + V_{th}}{R_g \frac{C_{iss}}{g_m} + L_s} \quad (4)$$

$$\frac{dV_{ds}}{dt} = \frac{V_{gs}}{R_g C_{gd}} \quad (5)$$

Where I_d is the current flows into the drain of the transistor, g_m is the transconductance of the device, C_{iss} is the input capacitance of the device, which is the sum of C_{gs} and C_{gd}, V_{th} is the threshold voltage of the semiconductor, V_{Miller} is the Miller voltage of the device. Take SiC MOSFTEs as an example, as shown in (2) to (5), with smaller input and output capacitance, a faster changing rate for drain current and drain to source voltage can be achieved. Experimental results can be found in Fig.2 [8].

Specifically, GaN HEMTs have a unique structure. The layer between AlGaN and GaN is a high-mobility electrons layer, also called "two-dimensional electron gas" (2DEG). The 2DEG provides a channel between drain and source. Thus, GaN HEMT is by natural a depletion-mode (normally on) device [2]. Although theoretically a normally-on device can also be used as power switches, but it requires a more complex driver design to realize that. To obtain a normally off device, several methods are proposed. Some of them proposed gate improvements [2], and enhancement mode GaN HEMT are manufactured and applied to various applications. Brought by the unique symmetric structure enhancement mode GaN HEMT, it possesses a reverse conduction characteristic, which could lead to divergent oscillation, causing high frequency noises [27], as shown in Fig.4. Others proposed a cascode structure, where a low power Si MOSFET is used to control a depletion mode GaN HEMT [23] – [26]. Although it has been presented in [23] [24], under zero voltage switching (ZVS), cascode GaN HEMT could reduce both conduction and switching loss, the complicated structure of cascode GaN HEMT itself could also lead to divergent oscillation [25]. The high frequency noises could seriously increase EMI emission.

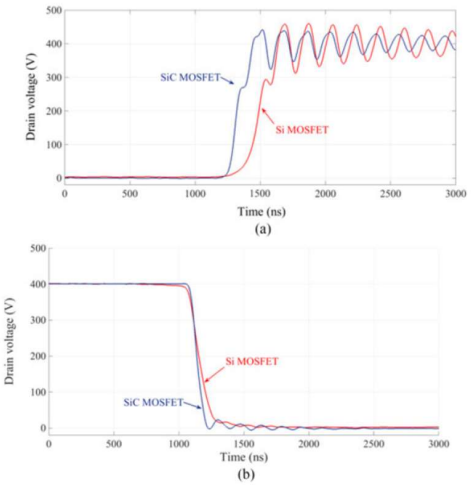


Fig. 2 Switching waveforms comparison between SiC MOSFET and Si MOSFET during turn on (a) and turn off (b) [8]

In a power semiconductor device, the on resistance is one of the most important factors. Given a drift region material, the on resistance of a device can be calculated as follows:

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot E_{crit}^3} \quad (6)$$

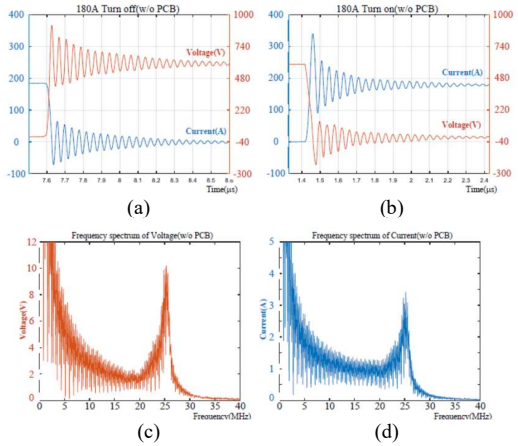
Where V_{BR} is the breakthrough voltage, ε_0 and ε_r are dielectric constant and permittivity, μ_n is the electron mobility and E_{crit} is the critical electric field.

As we can see from (6), the on resistance of power semiconductor made with WBG material could be much smaller than Si devices. As a result, much higher operation frequency could be achieved for WBG devices while satisfy the same efficiency requirements. It has been reported WBG devices could operates in several MHz for power rating higher than 10kW.

B. Characteristics of WBG devices as EMI noise Sources

We can see in Fig. 2, during turn on and turn off, overshoots and high frequency oscillations exist in both current and voltage waveforms. High frequency ringing in time domain waveforms could result in high spikes in the spectrum. Oscillations caused high frequency EMI was widely reported [6] [7] [28] - [31]. An example showed in Fig. 3 [30].

We can clearly observe a spike in the spectrum around 25MHz, which is the oscillation frequency. High frequency spectral components could be very difficult to filter out because high frequency performance of the EMI filters is limited by core materials and their own parasitic parameters [12].



(a) (b) (c) (d)

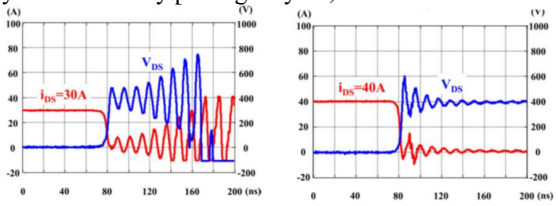
Fig. 3 (a) time domain waveform during turn off transition, (b) time domain waveform during turn on transition, (c) frequency spectrum of voltage, (d) frequency spectrum of current

Normally, high frequency oscillations are caused by parasitic parameters of device packages and circuit layouts. It was illustrated in [5] that the high switching speed and high operation frequency of WBG devices could push the spectral content of converter into a near radio frequency (RF) domain, the influence of parasitic components becomes increasingly serious. Thus, understanding the roles these parasitic parameters play during switching transient is very important, not only it could explain the mechanism of EMI noise production, but also provide insights of how to design counter measures to reduce EMI noise from sources. During switching transient, the turn on overshoot current and turn off overshoot voltage can be expressed as (7) and (8).

$$I_{max} = \sqrt{\frac{2Q_{rr}\frac{dI_d}{dt}}{S+1}} + I_L \tag{7}$$

$$V_{overshoot} = -(L_s + L_d) \cdot \frac{dI_d}{dt} \tag{8}$$

Where Q_{rr} is the reverse recovery charge of the diode in Fig.1. I_L is the load current and S is the snappiness of the diode. We can see that the overshoots are directly related to the loop inductance and diode parameter. To reduce the overshoots in current, a diode with smaller reverse recovery should be chosen. To reduce overshoot voltage, the parasitic inductance, which is mostly determined by package layout, must be reduced.



(a) (b)

Fig.4. Switching transition of cascode GaN HEMT [25]. (a) Divergent oscillation observed in cascode GaN HEMT with regular package during turn off, (b) no divergent oscillation was observed in cascode GaN HEMT with proposed package in Fig.5, during turn off.

If the parasitic parameters are not properly designed, high frequency oscillations could even be divergent and cause stability problems, as shown in Fig.4 (a). In [29], the instability issues were reported and analyzed for WBG devices in bridge structure, the unintended oscillator concept was proposed and perfectly described the divergent oscillation. Divergent oscillation in cascode GaN HEMT application was discussed in [25], detailed analysis was presented, and a solution was proposed to avoid divergent oscillation by adding an extra capacitor inside the device package. [27] analyzed instability issue for enhancement mode GaN HEMT, it is a unique behavior caused by the specific reverse conduction characteristics of enhancement mode GaN HEMT. The system was linearized and analyzed using modern control theory.

III. Package Design Techniques for EMI Reduction in WBG Devices Applications

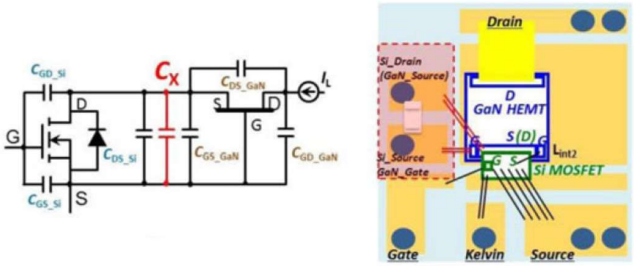
From (2) to (8), we can see that voltage and current overshoot and the oscillation during switching transient are determined by parasitic components including junction capacitances and parasitic inductances. With smaller junction capacitance, WBG devices are more sensitive with parasitic inductance. Methods in package designing to reduce parasitic inductance were proposed in various papers and reviewed in this Chapter.

A. Device Level Packaging

In device level packaging, multiple methods have been developed to reduce power loop and drive loop inductances brought by layout parasitic parameters. In [40], a method using near field scanning technique as guidance to reduce parasitic inductances were proposed for individual SiC MOSFET chips. Other methods including using additional Kelvin pin to reduce drive loop inductance, using surface mount package like island package or PQFN package to reduce parasitic inductance brought by terminal electrodes.

TABLE II. General Methods to Reduce Inductance [34]

Classification	Inductance Reduction Methods
DBC Substrate Pattern	1. Widen the pattern width 2. Shorten the pattern length
Bonding Wires	1. Shorten the wire length 2. Increase the number of Al wires 3. Increase the diameters of wires
Inductance of Electrode	1. Shorten the length 2. Increase the width 3. Parallel the main electrodes and reduce the space between the main electrodes 4. Use eddy current effect



(a) (b)

Fig.5. The proposed stacked die package for cascode GaN HEMT with compensating capacitor. (a) Schematic of the package and (b) Illustration of the layout of the stacked die package. Compensating capacitor is in the red shaded area [26]

Specifically, several package improvements were proposed in [23]-[26] for cascode GaN HEMT. In [26], a stacked die package with a compensating capacitor was proposed a shown in Fig.5. The stacked die design could reduce parasitic inductance of bond wires and the compensating capacitor is used to eliminate divergent oscillation and achieve ZVS. The value of this compensating capacitor can be calculated by (9).

Where Q_{III} is the total mismatched charge, as defined in [23]. V_A is the avalanche voltage of the drive MOSFET.

$$C_X \geq \frac{Q_{III}}{V_A - V_{TH\_GaN}} \quad (9)$$

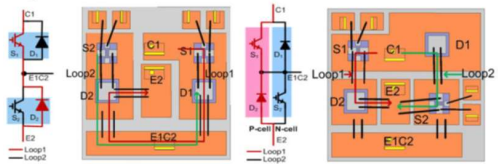
Multiple advantages were reported including the elimination of divergent oscillation [25]. With compensated mismatch charge, the depletion mode GaN HEMT in the cascode structure will no longer turn on unintentionally. With eliminated source, no divergent oscillation could happen, which is very beneficial for reducing EMI.

B. Module Level Packaging

Although device packaging could reduce parasitic inductance to some extent, the inductance of PCB trances, DBC (Direct Bond Copper) patterns and bond wires in power module is still large enough to cause high frequency oscillations and voltage and current overshoots. Multiple methods have been developed over the year to deal with parasitic inductances inside a power module. Typical methods were shown in TABLE II.

Other than the general methods listed in TABLE II, some papers proposed adding decoupling capacitors inside power module very close to power devices to reduce the area of current commutation loop. However, as a tradeoff, adding capacitors inevitably increase power loss and cost, also increase the complexity of the system.

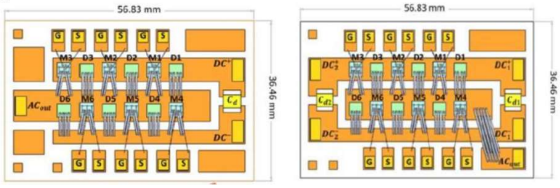
Other than adding capacitors, [34] proposed a P-cell and N-cell concept in power module design. By rearranging the position of device dies on the DBC of power modules, the area and length of current commutation loops are reduced, as shown in Fig.6.



(a) (b)

Fig.6. A Phase leg module layout. (a) Conventional arrangement and (b) Proposed arrangement with devices in the same switching cells close to each other [34]

As can be observed, with devices in the same switching cell put close to each other, the area and length of current commutation loop is greatly reduced compared to the conventional design. The parasitic inductance in the power loop is hence reduced. Although the original research was conducted on Si IGBT power module, the concept was later widely used in power modules with WBG devices [33].



(a) (b)

Fig.7. Illustration of power module layout of double end source design. (a) baseline layout and (b) double end source layout

A double end source design was proposed in [33] and further reduced the parasitic inductance. As shown in Fig.7. By a symmetrical arrangement, the trace length between power semiconductors were reduced and stray inductance is reduced accordingly.

In [35], a novel hybrid package was developed for SiC MOSFET power module. While bond wires still used to connect device dies and direct bond copper (DBC), other part of power module was a planar structure. The hybrid structure combined the low cost of bond wires and small stray inductance of planar structure.

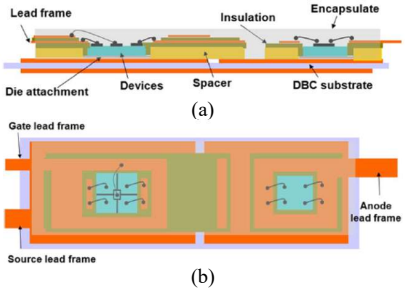
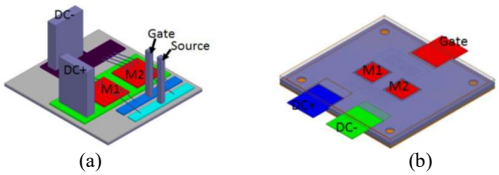


Fig.8. Hybrid Structure packaging proposed in [73]. (a) Side view and (b) top view

Besides the use of bond wires, different bonding techniques were developed over the years and promoting the use of planar module structure and 3D structure. Both experimental and simulation results showed reduced oscillations and EMI noises for power modules in planar structure. Comparisons were made in [15] for experimental result and [14] for simulation results. The wire bonded and wire bondless structures in [14] are shown in Fig.9. 3D structures proposed in [38] presented smaller stray inductance than wire bond structures. Although the PCB on DBC power module designed in [38] is for IGBT, the original purpose in the paper is to reduce stray inductance for WBG device applications. Also, the power chip-on-chip 3D concept is transferrable when designing power modules with WBG power semiconductors. Although results reported showed that planar structures and 3D structures presented better performance in both conductive [15] and radiated [14] EMI, the high cost and difficulties in manufacture process make them undesirable for some industry applications. In the above-mentioned studies, although multiple solutions were proposed to reduce parasitic inductance in the power module. The essential ideas are the same: reducing the inductance of the current traces by reducing the length and increasing the width.



(a) (b)

Fig.9. Illustration of wire bonded structure and integrated planar structure. (a) Wire bonded structure (b) wire bondless structure [14]

However, there are other methods that could reduce inductance: utilizing mutual inductance. [36] proposed a multiloop method for PCB design, by using interleaved multiloop, the magnetic flux generated by current loops could be canceled, the mutual inductance of the two loops are negative, thus reduce the parasitic inductance. Three kinds of multiloop layouts were proposed that could reduce both power loop and drive loop inductance. One of them is shown in Fig.10 as an example. The PCB layout is for a Buck converter with paralleled devices. The black arrows are current in the power loop. We can clearly see that the current direction is

opposite for each power loop. The mutual inductance between each loop is negative and thus reduce the total power loop inductance.

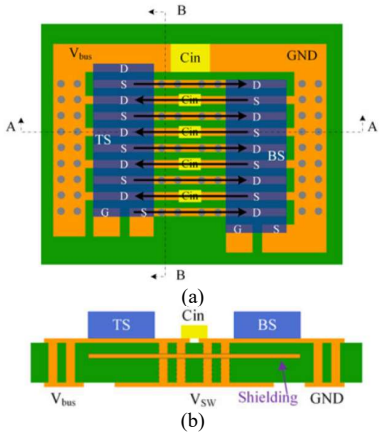


Fig.10. Example of proposed PCB layout using multiloop method. (a) Top view (b) Section view from A

Another power module design utilizing mutual inductance was described in [22]. A half bridge module applying SiC MOSFETs with improved hybrid packaging method was proposed. The drive loop inductance was analyzed and reduced reducing positive mutual inductance with proper placement of auxiliary source connection.

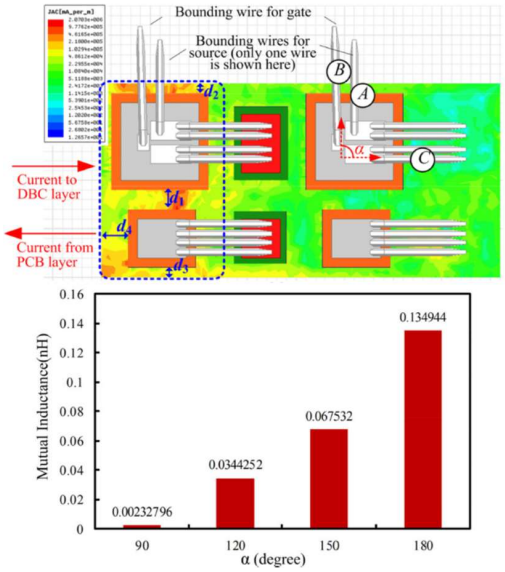


Fig.11. The auxiliary source connection is positioned 90 degrees with the rest of source connection, reducing positive mutual inductance between them [22]

Other methods could also be applied to reduce EMI for power electronics systems with WBG devices. Integrated CM capacitors were added inside the package in [10], providing in-module EMI filtering. As shown in Fig. 12. The common mode capacitors were integrated inside the module, providing filtering effect. `

Mostly in the above-mentioned research, the effectiveness of reduced stray inductance is verified by switching waveforms. However, the improvements in EMI is more straightforward in spectrum. One example is shown in Fig. 13. The measure total EMI noise for wire bonded and wire bondless packages in Fig.9 are shown in Fig.13. As can be observed, with reduced stray inductance, EMI noise is greatly reduced for wire bondless package.

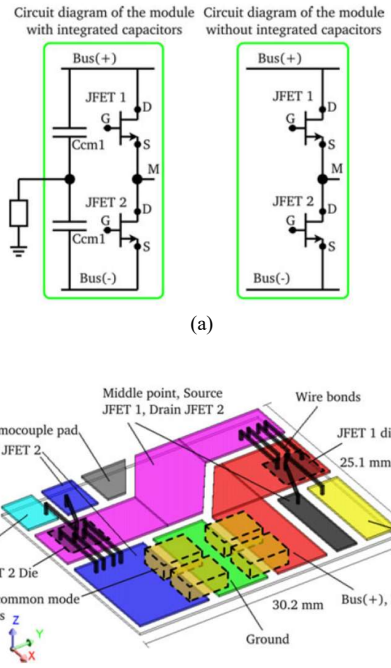


Fig.12. Illustration of in-module integrated CM capacitors. (a) Schematic (b) perspective view

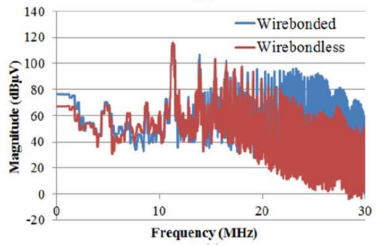


Fig.13. Measured conducted EMI for wire bonded and wire bondless package in Fig.9

IV. Conclusion

The superior properties of WBG materials could increase device switching speed, reduce power loss, and increase switching frequency. At the same time, these characteristics generate more severe high frequency noises than Si power devices. In this survey, properties of wide bandgap materials are reviewed, how EMI noises are worse for WBG power semiconductors were explained. After that, a detailed survey about reducing EMI by designing both device and power module packaging to reduce parasitic inductance were conducted. Various of package improvements were presented.

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